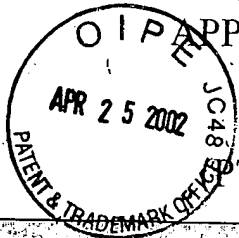


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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
<i>Loke</i>	4442652 A1	01/25/1996	German(w/English Abstract)				<input checked="" type="checkbox"/>

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>Loke</i>	Novel Selective Epi Base for double-poly Structures. In: IBM Technical Disclosures Bulletin, 1992, Vol. 35, Pages 51 - 53
<i>Loke</i>	PFIESTER, J.R.; SIVAN, R.D.; GUNDERSON, C.D.; CRAIN, N.E. (et al.): An ITLDD CMOS Process with Self-Aligned Reverse-Sequence LDD/Channel Implantation. In: IEEE Transactions on electron devices. ISSN 0018-9383. 1991, Vol. 38, No. 11, Pages 2460 - 2464
<i>Loke</i>	Substrate Contact with closed bottom Trenches. In: Research Disclosures, 1991, Vol. 322, No. 32246
<i>Loke</i>	Soft error rate reduction in Trench Technology. IBM Technical Disclosures Bulletin 1992, Vol. 34, No. 9, Pages 117 - 118
EXAMINER	<i>Loke</i>
DATE CONSIDERED	<i>5/21/02</i>

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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